35. The apparatus of claim 34, wherein said first through fourth pre-decoders use an inverse function of a generating function used for encoding.

36. The apparatus of claim 34, further comprising a first pre-processing unit preceding said second pre-decoder.

37. The apparatus of claim 36, further comprising a second pre-processing unit preceding said third pre-decoder.

38. The apparatus of claim 37, further comprising a third pre-processing unit preceding said fourth pre-decoder.

39. The apparatus of claim 38, wherein the first, second and third pre-processing units are implemented with a summer, a combiner or a selector.

40. The apparatus of claim 38, further comprising:

a selector which receives inputs from said first, second and third pre-processing units and an input having a full data rate and selects one according to an output from said decision unit; and

a Viterbi decoder which receives and Viterbi decodes only said selected output from said selector.--

REMARKS

Claims 1-40 are all the claims pending in the application. Claims 1,2, 4-10 and 12-26 have been amended to more clearly define the invention. Claims 27-40 have been added to more completely claim the invention. No new matter has been added.